Amendments To The Claims

The listing of claims presented below will replace all prior versions, and listings, of claims in the application.

Listing of claims:

1-13. (cancelled)

14. **(currently amended)** A synchronous memory device for synchronization of an external input clock with an internal input clock comprising:

a delay locked loop (DLL) having a clock divider,

a power down controller for determining a power down condition ~~based at least on a predetermined state of a clock enable signal inputted to the DLL~~,

wherein the clock divider outputs a first clock signal when the synchronous memory device is in the power down condition,

wherein the clock divider outputs a second clock signal when the synchronous memory device is in a non-power down condition, and

wherein a frequency of the first clock signal is lower than that of the second clock signal.

15. (original) The synchronous memory device of claim 14, wherein the frequency of the second clock signal is 2M when the frequency of the first clock signal is M.